AMENDMENTS TO THE SPECIFICATION

Page 1, first full paragraph:

Apparatuses and methods consistent with the ~~This~~ invention are ~~is~~ related to the acquisition of ~~acquiring a~~ fast and accurate estimations of the power requirement for a VLSI circuit, specifically to the creation and use of ~~a method for creating and using~~ core models of circuit elements incorporating instruction-level simulation coupled with gate-level energy analysis. In particular, the core models for the circuit elements are developed using object-oriented paradigms, and then instantiated into an overall device model, thereby allowing simulations of various device functions to be executed and the energy and power requirements of the device to be assessed. ~~The invention is embodied in a method, a computer system, and a computer program product that creates and uses object-oriented core models.~~

Page 7, third full paragraph:

The invention has been made in view of the above circumstances and the exemplary and non-limiting embodiments of the present invention may overcome the above disadvantages and other disadvantages not described above. However, the present invention is not required to overcome the disadvantages described above, and the exemplary and non-limiting embodiments of the present invention may not overcome any of the problems described above.~~has an object to overcome the above problems and limitations of the prior art, and has a further object to provide the capability to provide a method for power and energy estimations for simulated circuits, wherein the method includes the creation of core models.~~

Please delete the paragraph bridging pages 7 and 8.

Page 8, first full paragraph:

An aspect of the invention is ~~It is a further object of the invention to provide~~ a method and a computer program product for energy and power estimation for a SOC, wherein the energy and power estimates are calculated using core models.

Page 8, second full paragraph:

Another aspect of the invention is ~~It is a further object of the invention to provide~~ a method and a computer program product for implementing a core model that correlates simulated functionality to gate-level simulations of energy and power consumption.

Page 8, third full paragraph:

Another aspect of the invention is ~~It is a further object of the invention to provide~~ computer executable code for simulating the energy and power requirements of a SOC;

Page 8, fourth full paragraph:

Another aspect of the invention is ~~It is an object of the invention to provide~~ a class library, wherein the class library contains parameterized core models that can be instantiated into a simulation of a system design;

Page 8, fifth full paragraph:

According to an aspect of the invention, the circuit model incorporated into the core model may be ~~is~~ based upon a hardware description language.

Page 8, sixth full paragraph:

According to an aspect of the invention, ~~the invention provides~~ a plurality of instructions can be ~~that are~~ correlated to the functions of the circuit model in the core module.

Page 8, seventh full paragraph:

According to an aspect of the invention, ~~This invention allows~~ an object oriented client application may ~~to~~ construct an instance of a class for the purpose of representing the functions of a silicon circuit block that is included in a large scale integrated circuit.

Page 9, second full paragraph:

Preferably, but not necessarily, an aspect of the invention provides a method for energy and power estimation of a core-model based embedded system by capturing gate-level energy simulation data, deploying the captured gate-level simulation data in an algorithmic-level executable specification, wherein the captured gate-level data simulation data correlates to a plurality of instructions, and executing the algorithmic-level executable specification to obtain energy estimations for each instruction.

Page 9, third full paragraph:

Preferably, but not necessarily, an aspect of the invention ~~also~~ provides a method of modeling energy and power requirements for a system-on-a-chip by deploying a circuit model of the system-on-a-chip by selecting at least one parameterized instruction-based core model and instantiating the at least one parameterized instruction-based core model, executing the circuit mode, analyzing the estimated energy requirements of the circuit model, and outputting the estimated energy requirements for the circuit model.

Paragraph bridging pages 9 and 10:

Preferably, but not necessarily, an aspect of the invention provides a method for creating a library of instruction-based core energy models by deploying a circuit model using a hardware description language, defining a plurality of high-level instructions correlating to functions supported by the circuit model, acquiring gate-level energy simulation data for each component comprising the circuit model, collecting a plurality of toggle count sets corresponding to each of the plurality of high-level instructions, assigning each of the plurality of toggle count sets to one of the plurality of high-level instructions, thereby creating an instruction-based core energy model, and implementing the instruction-based core energy model within the library that is realized as a look-up table.

Page 10, first full paragraph:

Preferably, but not necessarily, an aspect of the invention also provides a computer program product for use in a computer system in which core models are accessed by an application program, the computer program product including a computer usable medium bearing computer executable code, including a first executable code portion for determining if the core model should simulate an idle state or execute an instruction, based upon whether the core model is called by another core model or it is called by a control object, a second executable code portion for determining if resources required by the core model are free, and claiming the free resources, a third executable code portion for adding an idle energy value to an energy accumulator, a fourth executable code portion for determining if a clock counter are decremented, thereby collecting data about the elapsed time and calculating the consumed power from the energy data, a fifth executable code portion for simulating execution of a predetermined instruction, and a sixth executable code portion for adding energy value to the energy accumulator.

Paragraph bridging pages 10 and 11:

Preferably, but not necessarily, an aspect of the invention provides a computer program product for use in a computer system in which core models are accessed by an application program, including a computer usable medium bearing computer programming statements for enabling the computer system to create at least one circuit model object for use by the application program, the computer programming statements including a class library expressing

an inheritance hierarchy and including at least one core model base class for constructing instances of a circuit model object, with the core model base class representative of a circuit element, the core model base class including, as a respective subclass thereof, an autonomous core model class defining at least one core model member function for directly interacting with the application program, and the core model member function simulating an instruction associated to the circuit element, the circuit element providing one-time predetermined data correlated to the simulated instruction.

Page 11, first full paragraph:

Preferably, but not necessarily, the invention ~~also~~ provides a computer system having an application program that models the energy and power requirements of a system-on-a-chip circuit design, with an energy and power modeling method for an application program to access and execute a parameterized core model of a circuit element, the method providing to the application program a circuit object representing a modeled circuit, with the circuit object having instantiated a parameterized core model having member functions for simulating functions assigned to circuit element, wherein the member functions output an energy and power estimation correlated with each simulated function, the application program sending a message to the circuit object to invoke the member functions, thereby executing a simulated function of the circuit element; and the circuit objects sending a message from the circuit object to the application program embodying the energy and power estimation with respect to the invoked member function.

Paragraph bridging pages 11 and 12:

An embodiment of the ~~The~~ invention may be ~~is~~ implemented using the C++ programming language, but any other object oriented language or environments capable of supporting its concepts, such as SMALLTALK, the MICROSOFT OLE/COM architecture, ~~and others~~ may be used as well. C++ has been chosen because it is widespread and therefore it easy convenient to make the concepts of this invention clear.

Please delete the first full paragraph of page 12.

Paragraph bridging pages 12 and 13:

The accompanying drawings, which are incorporated in and constitute a part of this specification illustrate embodiments of the invention and, together with the description, serve to explain the aspects ~~objects, advantages and principles~~ of the invention. In the drawings,

FIG. 1A is a block diagram illustrating modeling using method-calling;

FIG. 1B is a block diagram illustrating modeling using message-passing;

FIG. 1C is a block diagram illustrating modeling using structurally interfaced components;

FIG. 2 is a block diagram illustrating a prior art method of determining energy and power estimation for a simulated circuit;

FIG. 3 is a table depicting typical toggle counts for buffers of various sizes;

FIG. 4 is a block diagram illustrating an embodiment of the present invention;

FIG. 5 is a code fragment depicting the functions of a UART;

FIG. 6 illustrates a first embodiment for developing and using a core model according to the present invention;

FIG. 7 illustrates the process flow for refining the correlation between gate-level simulations and simulated instructions;

FIG. 8 illustrates a second embodiment for energy and power analysis for a circuit model using core models;

FIGS. 9A-9B illustrate the process flow for developing a core model according to the present invention;

FIGS. 10A-10B illustrate the process flow within a core model incorporating energy and power analysis for a core mode embodying a specified instruction set;

FIG. 11 illustrates an embodiment of a computer system;

FIG. 12 depicts a digital camera example illustrating the use of core models for the estimation of power and energy consumed by various simulated functions; and

FIG. 13 depicts the process flow for the energy and power analysis for a digital camera that is simulated with core models.

Please amend the heading on Page 13 as follows:

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

Page 13, first full paragraph:

Prior to describing the exemplary embodiments, ~~presently preferred embodiment of the invention,~~ some details ~~concerning the prior art~~ will be provided to facilitate the reader's understanding ~~of the invention and~~ to set forth the meaning of various terms.